D5BCA2201 **Reg. No.....**

Name: .....

FIFTH SEMESTER UG DEGREE EXAMINATION, NOVEMBER 2024

(Regular/Improvement/Supplementary)

BCA

GBCA5B07T: COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 2 Hours **Maximum Marks: 60**

SECTION A: Answer the following questions. Each carries *two* marks. (Ceiling 20 marks)

1. What are registers?
2. What is SR latch?
3. List any four memory reference instructions.
4. Differentiate between direct address and indirect address.
5. Explain the concept of associative memory.
6. Write short note on program control.
7. What is control memory?
8. Define cache memory.
9. Explain the concept of priority interrupts.
10. What is an opcode?
11. Distinguish between hardwired control and microprogrammed control.
12. What is Johnson's counter?

SECTION B: Answer the following questions. Each carries *five* marks. (Ceiling 30 marks)

13. What is a multiplexer? Design an 8x1 multiplexer.
14. Write a short note on stack organization.
15. Explain various addressing modes.
16. Give an account on DMA controller in detail.
17. Enumerate asynchronous data transfer in detail.
18. Explain the working of D and T flip flops.
19. Describe different types of shift registers.

SECTION C: Answer any *one* question. Each carries *ten* marks.

20. What is an instruction cycle? Describe various steps involved in an instruction cycle.
21. What is a decoder? Explain different types of decoders.

(1 × 10 = 10 Marks)