D5BCA2101 **Reg.No.....**

Name: .....

FIFTH SEMESTER UG DEGREE EXAMINATION, NOVEMBER 2023

(Regular/Improvement/Supplementary)

BCA

GBCA5B07T: COMPUTER ORGANIZATION AND ARCHITECTURE

Time: 2 Hours **Maximum Marks: 60**

SECTION A: Answer the following questions. Each carries *two* marks.

(Ceiling 20 Marks)

1. Draw the Logic diagram and truth table of Exclusive -OR gate.
2. What do you mean by Handshaking in Asynchronous data transfer?
3. Differentiate between Latches and Flip Flops.
4. What are Register Reference Instructions?
5. List out different types of Counters.
6. Mention the purpose of the instructions CLE and CLA.
7. Write a note on Edge triggering.
8. Comment on INPR and OUTR.
9. What is a Control Memory?
10. What are Decoders?
11. State the purpose of I/O bus.
12. Define Virtual Memory.

SECTION B: Answer the following questions. Each carries *five* marks.

(Ceiling 30 Marks)

13. Draw and explain the logic diagram and truth table of NAND,NOR gate.
14. Explain about BSA (Branch and Save Return Address) instruction.
15. For SR Latch using NAND gate, if S=0, R= 0 what will be the output? Justify the answer.
16. Write a note on Microprogram Routine.
17. Describe Parallel In Serial Out (PISO) Shift Register.
18. Write a note on Direct and Indirect addressing.
19. What are Multiplexers? Draw the circuit diagram and truth table of a 4X1 Multiplexer.

SECTION C: Answer any *one* question. Each carries *ten* marks.

20. Discuss about Design of Control Unit.
21. Explain different Cache mapping techniques in detail.

(1 x 10 = 10 Marks)