D1APH2404 **(3 Pages)** **Name.....**
Reg.No.....

FIRST SEMESTER M.Sc. DEGREE EXAMINATION, NOVEMBER 2024
(Regular/Improvement/Supplementary)

PHYSICS
FPHY1C04- ELECTRONICS

Time: 3 Hours **Maximum Weightage: 30**

Part A: Short answer questions. Answer *all* questions. Each carries *one* weightage.

1. Draw the device symbol of JFET, depletion and enhancement type MOSFET, all n-channel.
2. What is VVR and explain its working?
3. Relate Fill factor with efficiency of a solar cell. Explain the terms V_{oc} and I_{sc}.
4. What is the principle of working of tunnel diode? Why is it said to have negative differential resistance?
5. Differentiate between closed loop and open loop gain. Give the maximum attainable output voltage swing for a practical op-amp circuit.
6. What is a Karnaugh map? How many entries are there on a four variable Karnaugh map?
7. An op-amp can amplify both ac and dc voltages. Establish the statement with the help of frequency response curve for the op-amp.
8. What are charge coupled devices? Give any one application.

(8 × 1 = 8 weightage)

Part B: Essay questions. Answer any *two* questions. Each carries *five* weightage.

9. Explain the construction and working of semiconductor LASER. Discuss the method of population inversion, construction of optical cavity, method of feedback and achievement of the threshold current density in the LASER.
10. Elaborate on the op-amp parameters- Open loop gain,CMRR, power supply rejection ratio, input and output impedance, input offset voltage, input bias current, slew rate and UGB frequency.
11. Draw the circuit of an integrator circuit using op-amp and explain its working. Derive the expressions for frequency region where the integrator circuit works.
12. Describe the internal architecture of Intel 8085 microprocessor with the help of a neat diagram.

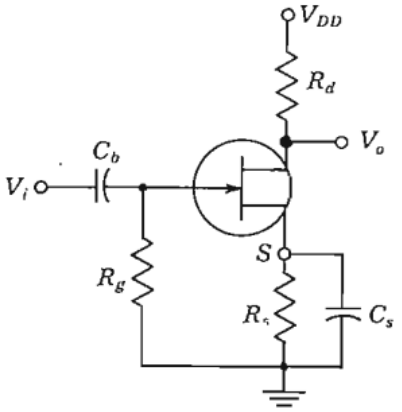
(2 × 5 = 10 weightage)

(P.T.O.)

Part C: Problems. Answer any *four* questions. Each carries *three* weightage.

13. Explain the V- I characteristics of an n channel JFET. Write down the expression relating I_{DS} and V_{GS} explaining the terms involved.

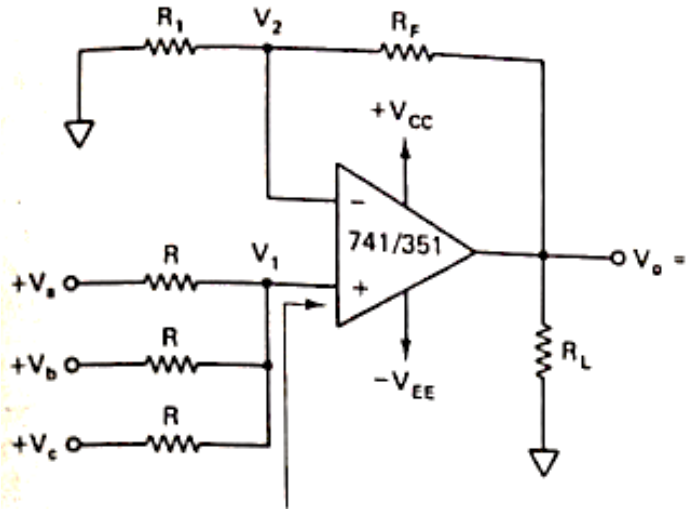
14. The amplifier in the figure utilizes an n-channel FET for which V_p = -2 V and I_{DSS} =1.65 mA. It is desired to bias the circuit at I_D= 0.8 mA, using V_{DD} =24 V. Assume r_d >> R_d. Find: a) V_{GS}; b) g_m; c) R_S; d) R_d, such that gain is at least 20dB, with R_S, bypassed by a very large capacitance C_S.



15. A silicon solar cell has an area of 100 cm^2 and is exposed to a solar irradiance of 1000 W/m^2. The short circuit current density (Jsc) of the cell is 35 mA/cm^2. Calculate the short circuit current (Isc) of the solar cell. Using this short circuit current, if an open circuit voltage (Voc) of 0.6 V, and a maximum power output (Pmax) is 1.2 W. Calculate the fill factor (FF) of the solar cell.

16. Draw the circuit of Wien Bridge oscillator and design for a frequency of 965 Hz.

17. In the circuit supply voltages = ±15V, V_a= +2V,V_b= -3V, V_c= +4V, R = R_1 = 1KΩ and R_F= 2KΩ. Determine the voltage V_1 at the non-inverting terminal and the output voltage V_o.



18. Show Karnaugh map for equation Y = F(A, B, C) = ∑m(1, 2, 3, 6, 7).

19. A D flip-flop has the following data sheet information: setup time= 5 ns; hold time = 10 ns; propagation time = 15 ns.

    a) How far ahead of the triggering clock edge must the data be applied?

    b) How long after the clock edge must the data be present to ensure correct storage?

    c) How long after the clock edge before the output changes?

(4 × 3 = 12 weightage)